

Development of Graphical Analytical Models for Digital Signal Processing System Structures

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Abstract— This paper proposes an improved method for describing digital filter structures as part of digital signal processing (DSP) systems, characterized by high information content of its models. The proposed approach is used to perform synthesis of graphical analytical models of DSP systems as well as their analysis by means of multilevel decomposition. All the system elements are presented in the form of functional structures, and the input counts processing - by the discrete system - is considered as the process of converting arguments by these functional structures. Moreover, graphical analytical models of basic structures of finite impulse response (FIR) and infinite impulse response (IIR) filters are developed and integrated with object-oriented programming language to be used in various projects in the form of snap-in modules. Additionally, the method, proposed in this paper is used for synthesising an optimized structure of a digital filter for calculating the mean and current values of determined periodic signal at the optimal discrete system's speed and invariance to discretization frequency. The obtained practical results show that the proposed method can be used with a great confidence in synthesizing optimized structures of digital filters as well as in the optimization of DSP systems' structures with the purpose of identifying the mean and RMS voltage values. The latter is an indicator that the proposed method can be applicable for various electronic systems.

Keywords— Digital signal processing; Graphical analytical model; Digital filter; Functional structure; Optimization.

1. INTRODUCTION

Digital signal processing (DSP) is of high fundamental and applicable value in electronics, telecommunications, modern radio engineering and the related fields. DSP methods are used for development and study of radio electronic devices and systems and its tools - are utilized for their hardware and software implementation. Modern electronic control systems as well as systems employed for information acquisition and processing are characterized with a large number of elements, numerous links and high volume of the processed data. Such systems widely use microprocessors with software-implemented algorithms of digital signals and data processing. Therefore, it is important for the electronic equipment developer to deeply understand the signal conversion processes, performed by the system, in order to develop the corresponding algorithms.

There is an increasing need for developing more complex digital systems within short periods of time and with minimum cost in order to become the first to launch the product. These requirements have revealed the limitations of traditional approaches - in designing the DSP systems - previously developed for small projects, in which the work at the component

level was a part of normal designing process. In more complex projects the work at the component level is no longer viable. This results in the need to work at a higher project abstraction level [1]. Here, the designer develops and utilizes high-level system models which are later implemented through circuit design with the use of the register logics, or through a software in the form of a source code in a high-level language (C/C++).

There are several equivalent forms for representing digital filters, linked with automatic control systems. These representations can be in the form a transfer function, difference equation, transfer function decomposition into common fractions, in a cascade form, in state-space representation and the Z-transform [2, 3]. In this case, the information about the DSP system structure is either unavailable or is presented in implicit form. Besides, description in the form of structural diagrams, schematic diagrams as well as modelling systems like Matlab/Simulink [4, 5], SciCos [6], Proteus, MultiSim, etc. are widely used, where the studied systems and their elements are represented with the use of various abstraction levels, obtained as a result of the primary system decomposition into individual subsystems [7]. Such subsystems convert input signals into output ones. However, the main disadvantage of such system descriptions is the lack of information about the structure of its individual elements, considered as a "black box". This causes difficulties in analysing the models adequacy as well as the practical implementation of signal processing algorithms. The description depth and detalization level are determined by the purpose of the system and are used for system model description. The study of peculiarities of this information is a subject of the system analysis [8].

High requirements are set to the digital filter parameters in the modern DSP systems [9, 10]. The orders of the filters frequently reach thousands and even higher. It results in the increase of calculation volumes and the soaring of hardware costs, and in case of software implementation of the digital filter it leads to high expenditure of processor time for all the necessary computations. During the digital filters synthesis the highest time and equipment expenditures are accounted for multiplication operations [11]. Therefore, the task of computation time minimization and the hardware costs reduction is accomplished by decreasing the number of multiplications that is necessary for computation of another filtered count [12]. In literature, the main attention is paid to the issues of parametric optimization of digital filters both in the processes of its designing based on analogue prototypes and in the development of adaptive filters [13, 14]. Therefore, the methods of DSP system structures' description need improvement, and, as is seen from the performed literature analysis, have substantial reserves for development.

The synthesis of the modern microprocessor control systems presupposes development of algorithms of processing the signals received from the primary instrument transducers. In this case, the direct transfer of the methods tested in the analogue control systems, to the digital systems, may sometimes be inefficient. Due to this fact, there also arises the issue of formal resolving of DSP system structure's synthesis for computing the mean and the mean square value of the determinate periodic signal at optimal discrete system speed considered by the author in [15]. Therefore, improving the DSP system and its individual elements description method as well as the use of digital filtration algorithms for improving microprocessor's information control quality, acquisition and processing systems operation is of high relevance. The approach to DSP systems description proposed in this paper extends

and supplements the methods of digital control systems structure description and the logical dynamic information transformation processes developed by the authors and presented in the works [16, 17].

The objective of the paper is the improvement of digital non-recursive and recursive filters structure description method used for building their graphical analytical models, in which all the elements are presented in the form of functional structures that perform the input arguments conversion that will provide the representation of DSP systems at various decomposition levels and implementation of formal approach to the solution of the task of their structural optimization.

In order to reach the set objective, it is necessary to:

- a) Analyze the operation of non-recursive and recursive filters from the viewpoint of various functional structures interaction and consider the processing of input count by the discrete system as the process of converting arguments by means of these functional structures.
- b) Develop the rules of formal description of DSP elements and present the structures of non-recursive and recursive filters in the form of graphical analytical expressions featuring with high information content.
- c) Develop an optimized structure of DSP subsystem for computation of mean square voltage value featuring with the number of computations independence for obtaining the output count from the input signal discretization frequency.

2. PRINCIPLES OF CONSTRUCTING GRAPHICAL ANALYTICAL MODELS FOR DIGITAL FILTERS

If the DSP subsystem input signal is considered as an argument and the output signal – as a function, then the subsystem will look like a certain functional structure. Therefore, the full description of the system may be presented in the form of interacting functional structures where each structure converts the input arguments. The first level of understanding the signal conversion processes is implemented for developer in the form of structural and schematic diagrams. The second level of understanding is intended for functional structure of microcontroller computing core, which is implemented in the form of computational mathematical models with input in converted arguments.

2.1. First Order Finite Impulse Response Filters Models

If the simplest schematic implementation of the first order low pass filter (LPF) with one zero on the basis of one time-delay element $Z^{-1} \rightarrow "f_1(\text{RS}Z^{-1})"$ is presented in the form of memory register and adder $f_1(\Sigma)$, written down in the form of graphical analytical expression as presented in the Fig. 1(a). Then this expression - taking in consideration the logical-dynamic arguments conversion process - may be written in the form of analytical expression as:

$$x(n) \rightarrow f(\text{Action}) \rightarrow y(n) \quad (1)$$

which adequately represents the arguments' conversion processes and fully complies with the concept of the functional structure by means of which the direct signal " $x(n)$ " and the delayed signal (or a number) from the delay element output are added. For memory register

functional structure, the “Action” is a one sampling period delay. Then, according to this presentation form, the delay element Z^{-1} will be indicated as “ $f_1(\text{RS}Z^{-1})$ ”, the summer is indicated as “ $f_1(\Sigma)$ ”, and the multiplier is indicated as “ $f_1(\Sigma)$ ” because - from the mathematical viewpoint - multiplication is a multiple addition. Supplementary information reflecting certain peculiarities of this element implementation is used in the indication of a functional structure performing time delay of sampled input signal for one clock cycle. In this case, it is indicated that the delay element is composed of RS-triggers. This trigger type is the basic type for building other types of triggers, in particular, D-triggers. In its turn, D-triggers form the basis for building memory registers, used in hardware implementation of delay lines in DSP systems. Therefore, the internal structure (theoretical structure) of the elements composing DSP becomes partially clear. Such elements in graphical analytical model are the “grey box”. The lower index in the indications corresponds to the ordinal number of the element in the digital filter structure.

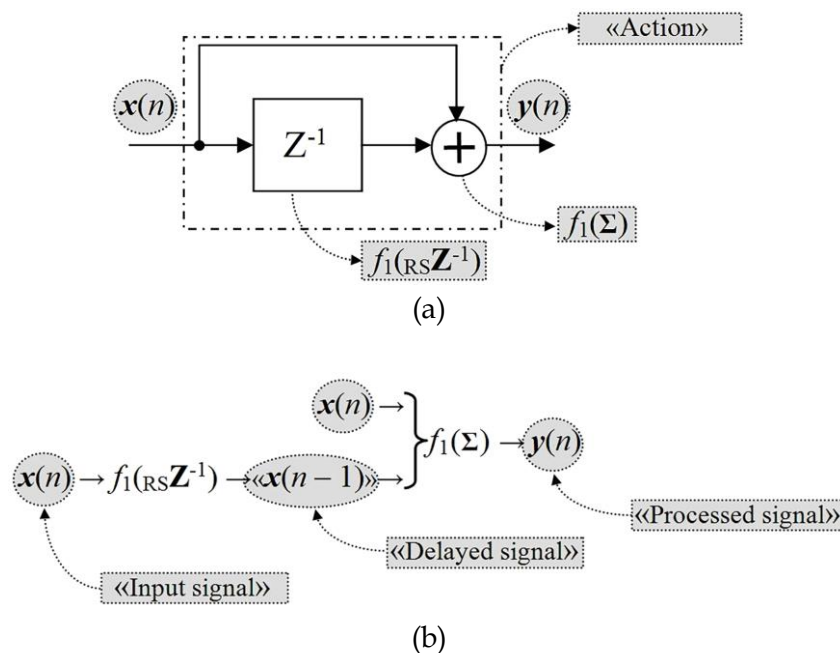


Fig. 1. a) The structure of hardware implementation of FIR-filter; b) graphical analytical expression describing the filter's functional structure.

If we return to the generally accepted mathematical representation of logical dynamic process of conversion of the graphical analytical expression input argument $x(n]$ (Fig. 1(a)), the operation of such low-pass filter will be described by the difference equation in the form:

$$y(n) = x(n) + x(n-1). \quad (2)$$

The order of this equation determines the order of the filter. The filter transfer function in the form of Z -transform will have the following form:

$$H(z) = 1 + z^{-1} \quad (3)$$

and the frequency and phase characteristics of this filter will be determined by the equations:

$$H(\eta) = 2 \cdot \cos(\pi \cdot \eta) \\ \arg[H(\eta)] = -\pi \cdot \eta \quad (4)$$

where $\eta = \frac{f}{f_s}$ is the relative frequency.

In analytical description of the digital filters structures, the symbol “}” of mathematical analysis is the “perfect” symbol. As specified in [18], it includes the functional structure content and may be specified with the use of various indices and symbols widely used in science. In this case such transition from the generally accepted form of mathematical model representation will be significantly simplified by the fact that the known forms of process description and representation include temporal sequence of signal conversion processes.

If the filter structure (see Fig. 1(a)) is presented in a form of analytical expression of Eq. (1), an analytical expression of the filter functional structure can be formulated as shown in Fig. 1(b). In this expression, unlike the difference equation (Eq. (2)), the source signal is the “Input Signal” which is subject to certain operations for “Processed Signal” $y(n)$ activation.

To extend the functions of such filter and the possibility of the transfer function modification, two multipliers - $f_1(\Sigma_\Sigma)$ and $f_2(\Sigma_\Sigma)$ - are introduced in the filter. They are used to introduce the coefficients b_0 and b_1 , written in the form of a graphical analytical expression shown in Fig. 2.

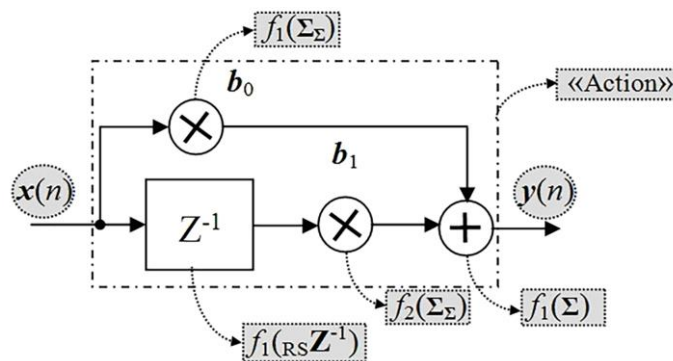


Fig. 2. The structure of hardware implementation of the digital FIR-filter.

Here, the difference equation, its Z-transform and transfer function will look as follows:

$$y(n) = b_0x(n) + b_1x(n-1),$$

$$Y(z) = b_0X(z) + b_1z^{-1}X(z), \tag{5}$$

$$H(z) = b_0 + b_1z^{-1}.$$

If the coefficients b_0 and b_1 are equal to 1, it is a LPF. If $b_0=1$, and $b_1=-1$, it is a high pass filter (HPF) [9].

If we write the filter structure - shown in Fig. 2 - in the form of graphical analytical expression as in Eq. (5), it is possible to form a functional structure of the analytical expression as presented in Fig. 3, where, unlike the difference equation (Eq. (5)), the source signal is the “Input Signal” which is subject to certain operations for “Processed Signal” $y(n)$ activation.

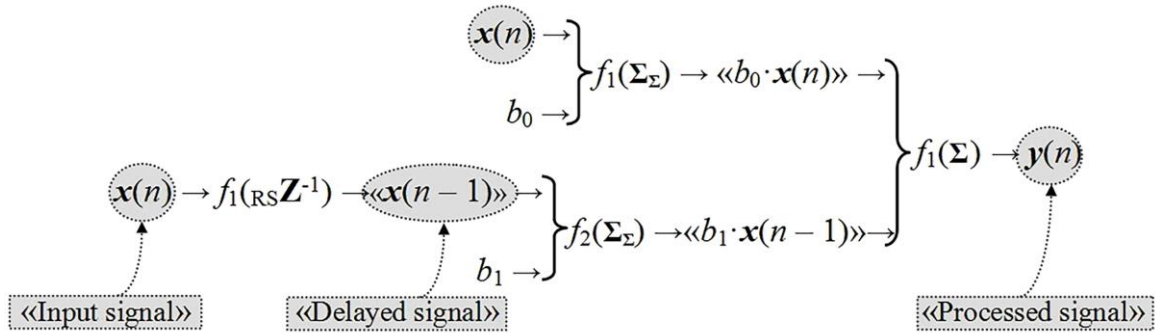


Fig. 3. Graphical analytic description of the FIR-filter functional structure.

2.2. First Order Infinite Impulse Response Filters Model

The second variant of the first order LPF/HPF design with one pole is presented in the form of a structural diagram in Fig. 4.

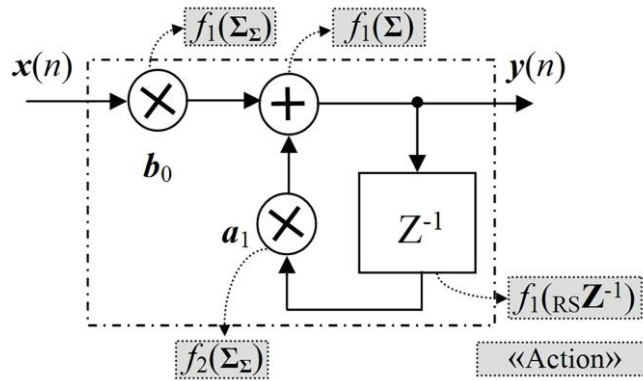


Fig. 4. Structure of the recursive digital filter's hardware implementation.

This filter diagram with the infinite impulse response (IIR) uses the feedback by means of which the direct and delayed signals are summarized; therefore, in the difference equation a term - with a negative sign and a coefficient a_1 - occurs:

$$y(n) = b_0x(n) + a_1y(n-1) . \tag{6}$$

Z-transform of this difference equation and its transfer function are determined by the equations:

$$Y(z) = b_0X(z) + a_1z^{-1}Y(z),$$

$$H(z) = \frac{b_0}{1 - a_1z^{-1}} . \tag{7}$$

For this filter structure, if $a_1 > 0$, it is LPF, if $a_1 < 0$, it is HPF. This filter has a pole at $z = -a_1$ both in LPF, and in HPF mode, the filter has zero at $z = 0$.

If we write the filter structure - shown in Fig. 4 - in the form of a graphical analytical expression as in Eq. (1), then, instead of algebraic expression presented in Eq. (6), it is possible to form a graphical analytical description of a functional structure, as presented in Fig. 5. In this expression, unlike the difference equation (Eq. (6)), the source signals are the "input signal" and "delayed feedback signal" which are subject to certain operations for the "processed signal" $y(n)$ activation.

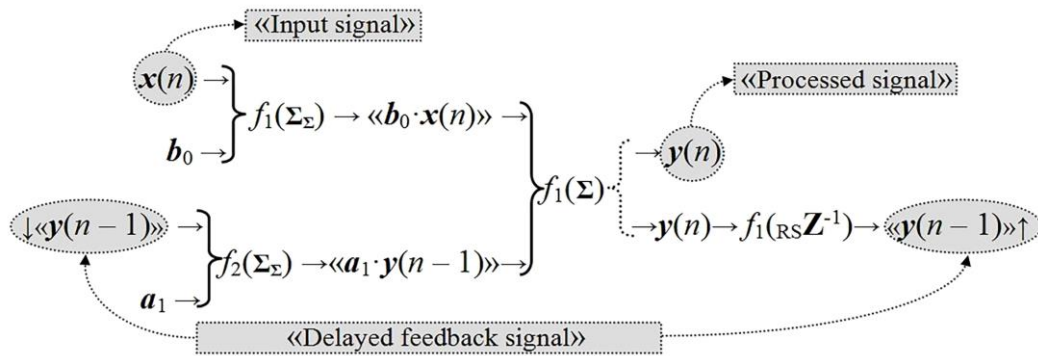


Fig. 5. Graphical analytical description of IIR-filter functional structure.

The considered principles of graphical analytical description of the simplest finite impulse response (FIR) and IIR filters will be used to describe the structures of digital filters of higher orders.

2.3. Second Order Infinite Impulse Response Filters Models

The second order filter with two poles consists of two links – the first order LPF/HPF with the use of two feedbacks represented in the form of graphical analytical expression shown in Fig. 6.

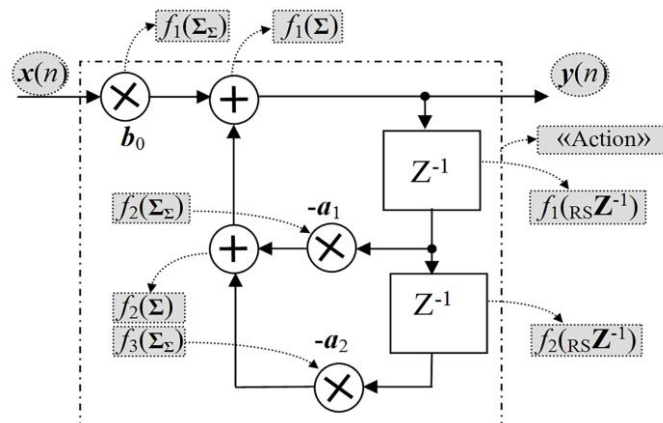


Fig. 6. Second order digital IIR-filter with two poles.

Difference equation, Z-transform and transfer function of this filter are described by equations as [9]:

$$y(n) = b_0x(n) - a_1y(n-1) - a_2y(n-2),$$

$$Y(z) = b_0X(z) - a_1z^{-1}Y(z) - a_2z^{-2}Y(z), \tag{8}$$

$$H(z) = \frac{b_0}{1 + a_1z^{-1} + a_2z^{-2}}.$$

If $(a_1 / 2)^2 > a_2$, these equations are possible to be represented in the following form:

$$y(n) = b_0x(n) + [2R \cos(\theta_c)] \cdot y(n-1) - R^2 \cdot y(n-2),$$

$$H(z) = \frac{b_0}{1 - 2R \cos(\theta_c) \cdot z^{-1} + R^2 \cdot z^{-2}} \tag{9}$$

where $R = \sqrt{a_2}$, $R < 1$, $\cos(\theta_c) = -\frac{a_1}{2R}$. Such conversion makes it possible to assign the cut-off frequency. If $\eta_c > 0.25$, it is an LPF; if $\eta_c < 0.25$, it is an HPF; at $\eta_c = 0.25$, the filter becomes resonant. The value R performs a damper function in this filter.

If we represent the filter structure – shown in Fig. 6 - in the form of graphical analytical expression as in Eq. (1), then, instead of algebraic expression in Eq. (8), it is possible to form a graphical analytical expression of the functional structure, presented in Fig. 7. Data transfer direction is displayed by the arrow (\uparrow). The input informational flow is indicated by the downwards arrow (\downarrow).

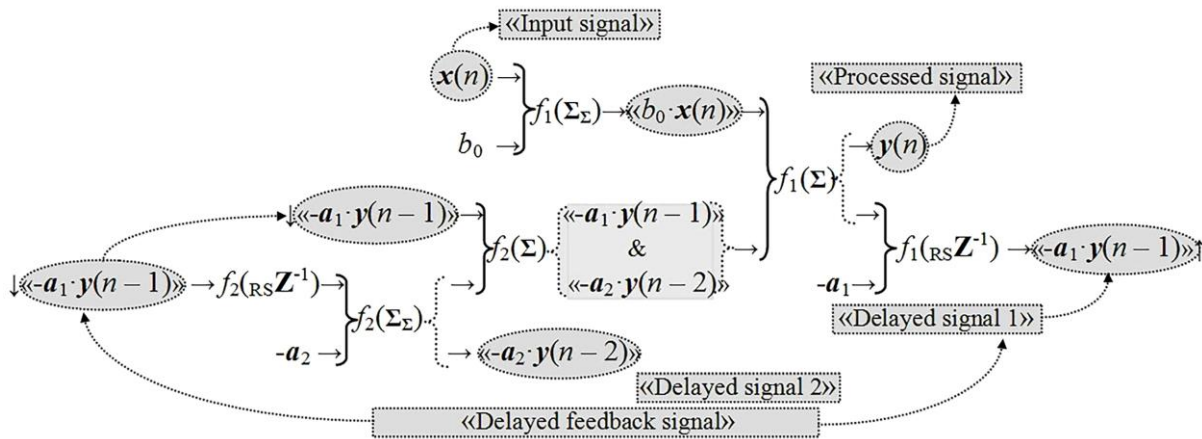


Fig. 7. Graphical analytical description of the digital IIR-filter functional structure.

Now we can form a functional structure of a graphical analytical model for the second order recursive filter (biquad filter), which is presented in Fig. 8. From the analysis of the generated graphical analytical structure we can see that the digital filter structure has five multipliers, four adders and two delay lines which are the memory registers. Besides, there is an analytical presentation of mathematical operations performed by the system elements at the input arguments and the interrelation between them.

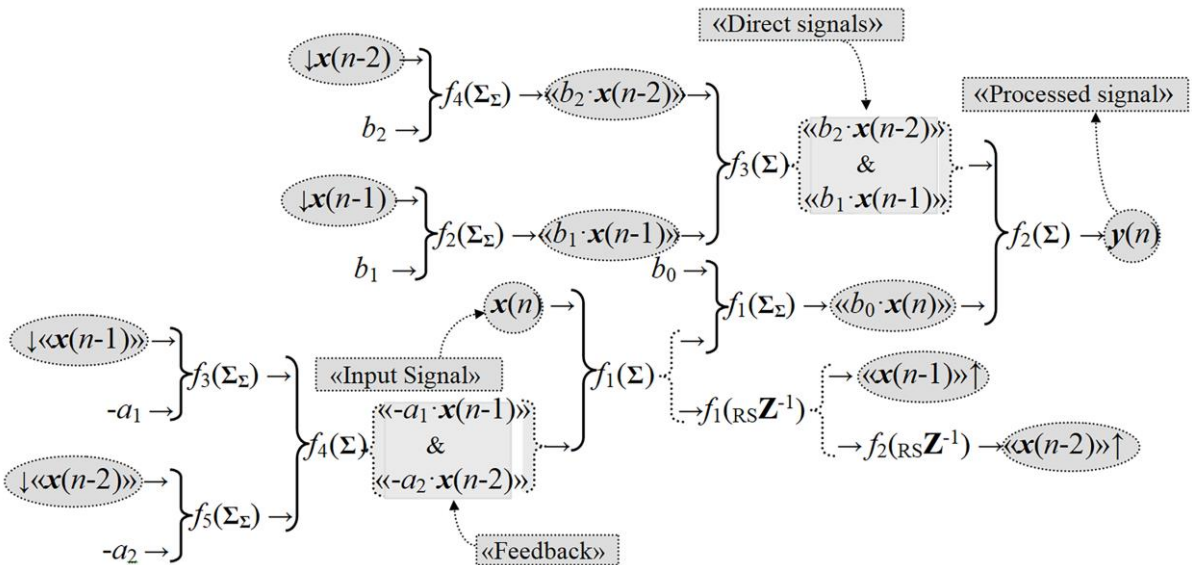


Fig. 8. Graphical analytical description of the biquad filter.

It is seen that it is possible to increase the filter's speed due to the parallel execution of the computation processes. In particular, the multiplication procedures that are performed by the functional structures of the multipliers f_2, f_3, f_4, f_5 , can be accomplished in parallel when the algorithm is executed at a multi-core processor, which should be taken in consideration during the program implementation of the filter. Filter structure presentation in the form of structural diagrams or difference equations precludes from such conclusions. Besides, the summarization operations by the adders f_3 and f_4 can be performed in parallel.

2.4. Optimized Structure of A System for Calculating Periodic Signals' Mean Value

The above-considered graphical analytical models of the basic structures of digital non-recursive and recursive filters are the "building blocks" of more complex DSP structures. The integration of the obtained models with the object-oriented programming language makes it possible to use them in the form of build-in modules in various projects.

Quite often, the task of digital filter optimization is to find the necessary weight coefficients at which the filter characteristics satisfy a certain quality criterion [9, 11, 18]. In this case it means parametric optimization of DSP systems. Structural optimization tasks can be solved by the developers intuitively, and is based on the accumulated experience. However, the resulting structure will not be optimal in all cases. The approach proposed in this paper may be used for formal approach to solution of DSP systems structural optimization, in particular, for synthesis of digital filter optimized structure for mean square voltage value computation. The arithmetical mean of variable signal $u(t)$ with period T is calculated according to the well-known mathematic formula:

$$u_{avg} = \frac{1}{T} \int_0^T |u(t)| dt \quad (10)$$

which can be written in the form of graphical analytical model presented in Fig. 9.

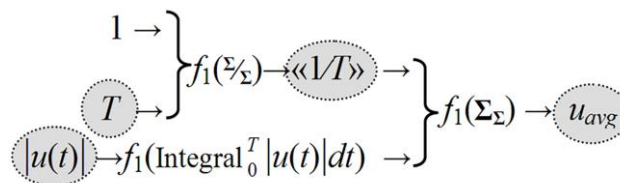


Fig. 9. Graphical analytical model of a periodic signal integration process.

A continuous input signal can be converted into a sequence of discrete values, if an input signal value is taken by means of sample-and-hold element in equal time intervals $t_n = n \cdot T_s$. Here $f_s = \frac{1}{T_s}$ is the sampling frequency. Then the expression for the periodic mean value (arithmetical mean) calculation can be presented in discrete form by:

$$u_{avg}(t) = \frac{1}{N} \sum_{n=0}^{N-1} |u(t - nT_s)|, \quad (11)$$

where $N = \frac{T}{2 \cdot T_s}$.

The expression in Eq. (11) can be written in the form of a graphical analytical model presented in Fig. 10.

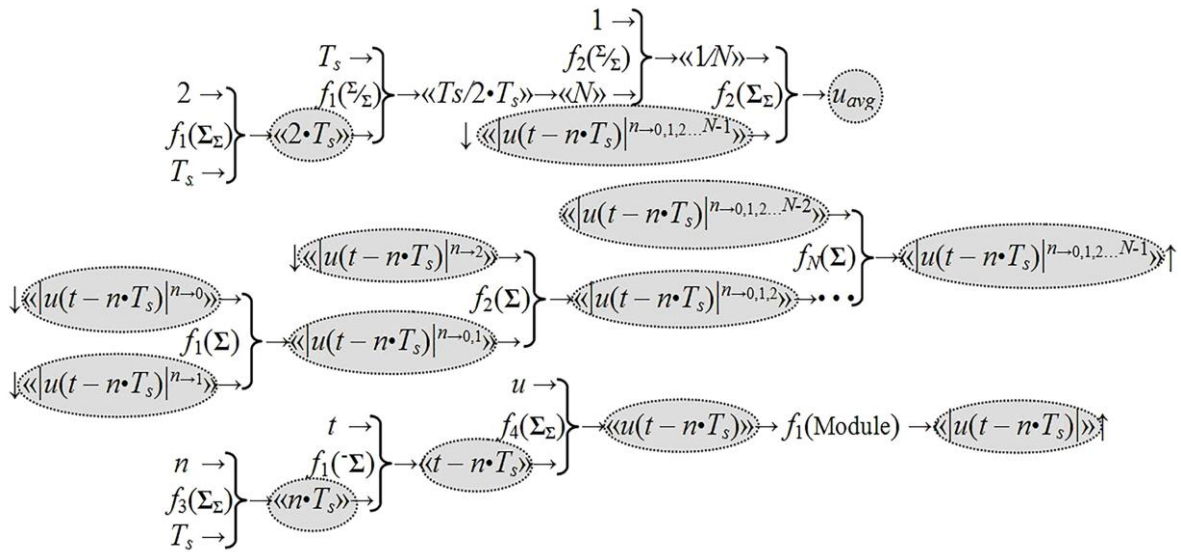


Fig. 10. Graphical analytical model of a system for calculation of the periodic signal mean value.

Let's introduce the designations $Y = u_{avg}$, $X = |u|$ into the discussion. After rewriting Eq. (11), putting the constant $\frac{1}{N} = h$ under the sum sign and moving to discrete time, the following expression is obtained:

$$Y(kT_s) = \sum_{n=0}^{N-1} h \cdot X[(k-n)T_s]. \tag{12}$$

Consequently, for activation of the final resulting argument $Y(kT_s)$ of the expression in Eq. (12), it is necessary to perform the input arguments conversion in compliance with the graphical analytical model presented in Fig. 11.

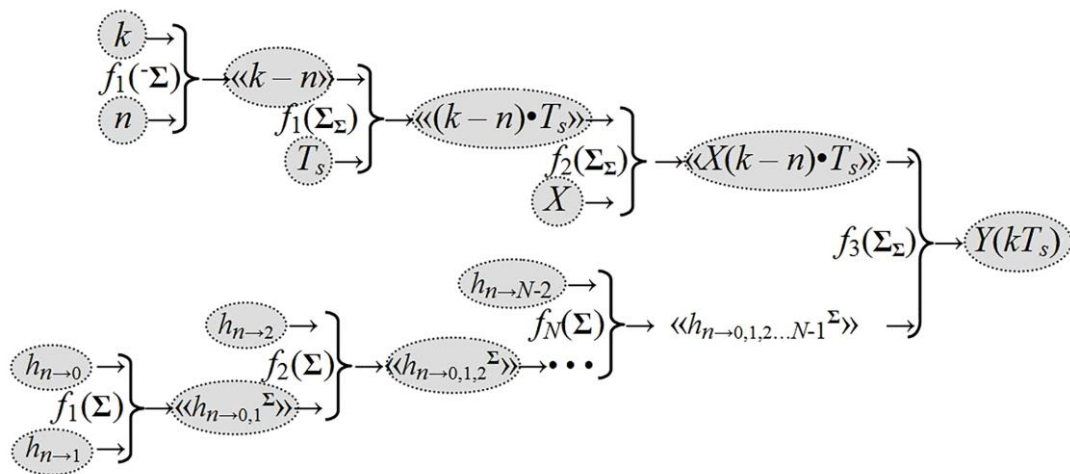


Fig. 11. Graphical analytical model of a digital filter structure for computation of the periodic signal mean value.

The presented graphical analytical model describes the structure of a linear filter with the final length impulse response $N - 1$ as shown in Fig. 12.

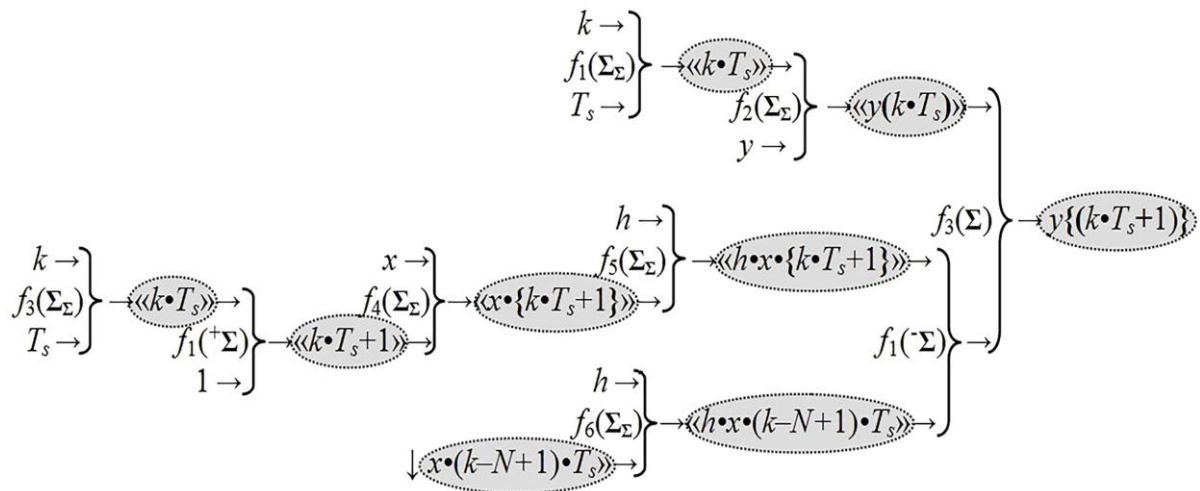


Fig. 12. Graphical analytical model of a digital filter's optimized structure for computation of a periodic signal mean value.

For computation of another output count of an optimized digital filter, it is necessary to perform three summation operations and one multiplication operation versus N summation operations and N multiplication operations in the basic filter structure. The payback for the smaller number of arithmetic operations is the increased length of the digital delay line by one memory element and allocation of an extra memory element for storage of intermediate result. If we introduce supplementary functional blocks A^2 and \sqrt{A} , the optimized structure of a digital filter for calculation of the input voltage average value with equal weight coefficients can be used for computation of an input voltage mean square value.

2.5. Results and Discussion

The optimized digital filter structure for calculating the average value of the input discrete signal, proposed in this paper and shown in Fig. 12, was implemented programmatically in the C programming language. A software implementation of the basic structure of such a filter before its optimization (as shown in Fig. 11) was also made to perform a comparative analysis of their effectiveness for different values of the filter order. In these structures of digital filters, there are no feedbacks. Therefore, they relate to linear stationary digital filters with FIR. The impulse response of an N^{th} -order FIR filters lasts exactly $N+1$ samples. The experiment was carried out using an ATmega128 microcontroller operating from an external generator with a clock frequency of 8 MHz. This microcontroller has a built-in 10-bit analog-to-digital converter. This bit depth will have the data received at the input of each of the filters. However, in this experiment, a step function (Heaviside function) was applied to the input of the filters to determine the value of the time interval required by the digital filters to perform all calculations and form the output value. The experiment was carried out for different values of digital filter orders – 16, 32, 64, 128, 256, 512, and 1000. Image Craft ICCAVR Version 7.22C was used as a compiler. Modelling the operation of the filters and determining the execution time of DSP algorithms were

performed using AVR Studio 4.12. The data obtained as a result of the experiment are presented in Table 1.

Table 1. Experimental results of digital filters' performance test.

Filter order	T_1 [us]	T_2 [us]	T_1 / T_2
16	271	180	1.51
32	423	240	1.76
64	727	360	2.02
128	1335	600	2.22
256	2549	1077	2.37
512	4980	2037	2.44
1000	9615	3866	2.49

Fig. 13 depicts the calculation time taken by digital filters to form an output value. It reveals that for small digital filter orders, the difference in the calculation time for the basic and the optimized filter structures are not significant. However, with an increase in the order of the filters, the difference in the time of performing the necessary calculations increases.

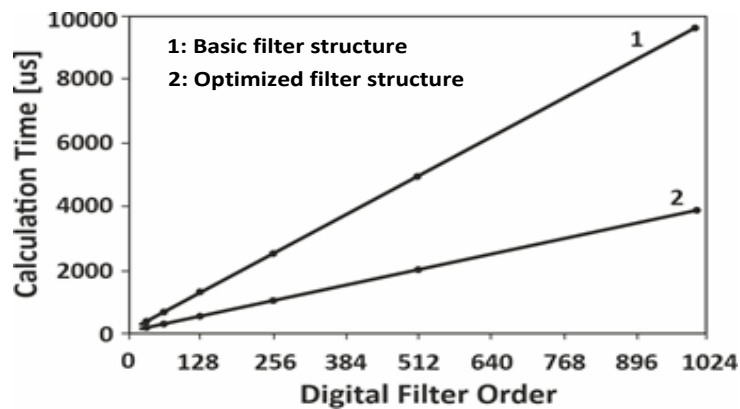


Fig. 13. Dependences of the output signal calculation time on the order of digital filters.

Fig. 14 shows the change in the runtime ratio (T_1/T_2) of the algorithm for calculating the average value of the input signal by the proposed filter with an optimized structure.

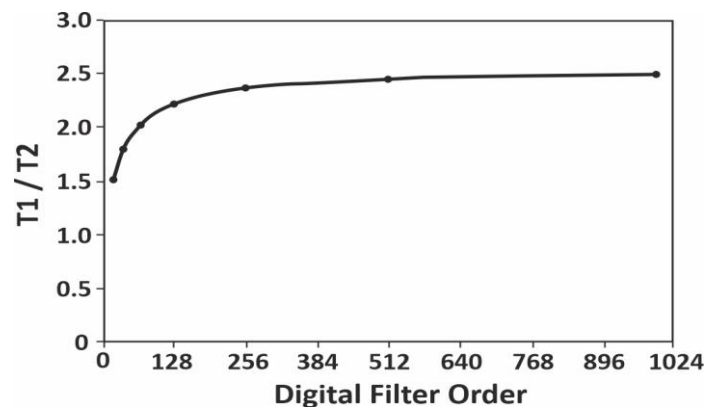


Fig. 14. Ratio of the output samples' calculation time, taken by the digital filters of the optimized structures.

It shows that the efficiency of the considered optimized digital filter is non-linear and depends on the order of the filter. For small values of the digital filters order, their performance is almost the same, however, with an increase in the order of the filters, the efficiency of the filter with an optimized structure sharply increases. This is important, since the considered algorithm is intended for implementation in 8-bit microcontrollers with RISC architecture, which are widely used in control and automation systems, rather than specialized signal processors. Such microcontrollers usually operate at low frequencies that usually amount to several tens of MHz, in contrast to specialized signal processors that are specifically designed to implement DSP algorithms with support of MAC operations at the hardware level. Thus, the time taken to calculate the average value of a discrete periodic signal by the optimized high-order digital filter, proposed in this paper, is up to 2.5 times less than the time required to perform all the calculations with a non-optimized filter.

The response time of the proposed digital filter's optimized structure, implementing the calculation algorithm of the voltage arithmetical mean, depends on the filter order. However, the increase of sampling frequency in the optimized filter structure does not result in greater number of arithmetic operations of addition and multiplication which is an advantage of the suggested filter structure in comparison with the similar ones. If the digital filter delay line length does not coincide with the number of samples in one period of periodic signals, oscillations will be observed in the signal at the filter output.

The use of microprocessor equipment and software implementation of computation algorithms will allow to exclude this phenomenon by means of correction of the digital filter delay line length depending on the input signal frequency. It gives the developed system the feature of adaptability to the input signal frequency deviations, which is not typical for similar systems.

3. CONCLUSIONS

An improved method of digital filter structures' description was considered in this paper. This method relies on the generation of a graphical analytical form of writing the informational arguments conversion procedure in the functional structures. Such approach provides improvement of informational content of mathematical subsystems of DSP systems by means of its decomposition. In its turn, it provides the assessment of the quality of its structure and elements from the general systemic approach viewpoint which simplifies integration testing of DSP system due to formal identification of all the possible schemes of hardware-software tool interaction. The practical value of the obtained results is the possibility of formal solution of the task of the digital filters optimized structures synthesis. The use of the suggested method provides DSP system structure optimization for identification of the arithmetical mean and RMS voltage value which can be used in various electronic systems.

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